CLAIMS

What is claimed is:

1. A memory system, comprising:

a plurality of rows, each row receiving identical input bits, each row having identical stored bits, each row generating, at a row output, a row hit signal when its stored bits match the input bits, and the row outputs are logically combined to generate a system hit signal when at least one of the rows generates a row hit signal.

2. The memory system of claim 1, where each row in the plurality of rows is in a different memory.

3. The memory system of claim 1, where at least two of the rows in the plurality of rows are in one memory.

4. The memory system of claim 1, where the system hit signal is a logical OR of the row hit signals.

5. A computer system, comprising:

a cache memory; and

a content addressable memory associated with the cache memory, the content addressable memory receiving input bits, the content addressable memory storing a plurality of copies of at least part of an address for each data item in the cache memory, the content addressable memory generating a signal indicating a match to the input bits when at least one of the plurality of copies of at least part of an address for each data item in the cache memory matches the input bits.

6. A method, comprising:

receiving, by a memory system, input bits;

comparing, by the memory system, the input bits to a plurality of identical sets of stored bits; and

generating a signal indicating a match when at least one of the identical sets of stored bits matches the input bits.

7. A content addressable memory system, comprising:

means for storing a plurality of copies of stored bits;

means for comparing each copy of stored bits to input bits; and

means for generating a system hit signal when at least one the plurality of copies of stored bits matches the input bits.

8. A memory system, comprising:

a plurality of rows, each row receiving identical input bits, each row having identical stored bits, each row generating, at a row output, a signal indicating whether its stored bits match the input bits, and the row outputs are logically combined to generate a system output signal corresponding to at least half of the signals from the row outputs.

9. The memory system of claim 8, where the row outputs are logically combined to generate a system output signal corresponding to a majority of the signals from the row outputs.